

What is claimed is:

- 1 1. A memory system comprising:
 - 2 a memory controller having an interface that includes a plurality of memory
 - 3 subsystem ports including a first memory subsystem port;
 - 4 a first memory subsystem including:
 - 5 a buffer device having a first port and a second port, and
 - 6 a plurality of memory devices coupled to the buffer device via the second
 - 7 port;
 - 8 and
 - 9 a plurality of point-to-point links, each point-to-point link having a connection to
 - 10 a respective memory subsystem port of the plurality of memory subsystem ports, the
 - 11 plurality of point-to-point links including a first point-to-point link connecting the first
 - 12 port to a first memory subsystem port to transfer data between the plurality of memory
 - 13 devices and the memory controller.
- 1 2. The memory system of claim 1 further including a plurality of connectors
 - 2 each connected to a connection to a respective point-to-point link and a plurality of
 - 3 memory subsystems, each memory subsystem of the plurality of memory subsystems
 - 4 including:
 - 5 a buffer device having a first port and a second port, wherein the first port is
 - 6 coupled to a respective connector of the plurality of connectors , and
 - 7 a plurality of memory devices coupled to the buffer device via the second port.

1 3. The memory system of claim 2 further including a plurality of substrates
2 wherein each memory subsystem is disposed on a respective substrate of the plurality of
3 substrates.

1 4. The memory system of claim 1 wherein each of the plurality of point-to-
2 point links, first memory subsystem, and memory controller include a common substrate.

1 5. The memory system of claim 1 wherein the first memory subsystem
2 further includes a plurality of channels and a plurality of memory device select lines
3 connected between the plurality of memory devices and the second port.

1 6. The memory system of claim 5 wherein each channel includes a plurality
2 of terminated signal lines.

1 7. The memory system of claim 1 wherein the buffer device of the first
2 memory subsystem further includes at least one selected from the group consisting of a
3 cache, a clock generator, and a clock alignment circuit.

1 8. The memory system of claim 1 further including a plurality of sideband
2 signals coupled between the plurality of memory devices of the first memory subsystem
3 and the controller device.

1 9. The memory system of claim 1 further including a plurality of sideband
2 signals coupled between the plurality of buffer devices and the controller device.

1 10. A memory system comprising:
2 a controller device;

3 a first buffer device having a first interface and a second interface;
4 a second buffer device having a first interface and a second interface;
5 a first point-to-point link having a first connection to the controller device and a
6 second connection to the first interface of the first buffer device;
7 a first channel connected to the second interface of the first buffer device;
8 a first plurality of memory devices electrically coupled to the first channel;
9 a second point-to-point link having a first connection to the controller device and
10 a second connection to the first interface of the second buffer;
11 a second channel connected to the second interface of the second buffer device;
12 and
13 a second plurality of memory devices electrically coupled to the second channel.

1 11. The memory system of claim 10, wherein the first buffer device, first
2 channel and first plurality of memory devices are disposed on a first substrate, and the
3 second buffer device, second channel, and second plurality of memory devices are
4 disposed on a second substrate.

1 12. The memory system of claim 11, further including a plurality of
2 termination elements disposed on each of the first and second substrate, wherein a first
3 plurality of termination elements are connected to the first channel, and a second plurality
4 of termination elements are connected to the second channel.

1 13. The memory system of claim 10, wherein the first buffer device further
2 includes a third interface, the memory system further including:
3 a third buffer device having a first interface and a second interface;

4 a third point-to-point link having a first connection to the third interface and a
5 second connection to the first interface of the third buffer device;
6 a third channel connected to the second interface of the third buffer device; and
7 a third plurality of memory devices electrically coupled to the third channel.

1 14. The memory system of claim 10 further including a third point-to-point
2 link having a connection to the controller and a fourth point-to-point link having a
3 connection to the controller.

1 15. The memory system of claim 10 further including:
2 a third channel connected to the second interface of the first buffer device;
3 a third plurality of memory devices electrically coupled to the third channel;
4 a fourth channel connected to the second interface of the second buffer device;
5 and
6 a fourth plurality of memory devices electrically coupled to the fourth channel.

1 16. The memory system of claim 15 further including:
2 a fifth and sixth channel connected to the second interface of the first buffer
3 device;
4 a fifth plurality of memory devices electrically coupled to the fifth channel; and
5 a sixth plurality of memory devices electrically coupled to the sixth channel.

1 17. The memory system of claim 10, further including at least one termination
2 element disposed on the first buffer device and electrically connected to the first point-to-
3 point link.

1 18. The memory system of claim 10 wherein the first and second buffer
2 devices each further include at least one selected from the group consisting of a cache, a
3 clock generator and a clock alignment circuit.

1 19. A memory system comprising:

2 a controller device;

3 a first and second plurality of buffer devices, each buffer device of the first and
4 second plurality of buffer devices having an interface connected to a respective plurality
5 of memory devices;

6 a first and second repeater device;

7 a first point-to-point link having a first connection to the controller device and a
8 second connection to the first repeater device;

9 a second point-to-point link having a first connection to the controller device and
10 a second connection to the second repeater device;

11 a first plurality of repeater links, each repeater link having a first connection to a
12 respective buffer device of the first plurality of buffer devices, and a second connection
13 to the first repeater device; and

14 a second plurality of repeater links, each repeater link having a first connection to
15 a respective buffer device of the second plurality of buffer devices and a second
16 connection to the second repeater device.

1 20. The memory system of claim 19, wherein each buffer device of the first
2 and second plurality of buffer devices and corresponding plurality of memory devices are
3 each disposed on a one of a plurality of respective module substrates.

1 21. The memory system of claim 19 further including a third point-to-point
2 link having an end connected to the controller and a fourth point-to-point link having an
3 end connected to the controller.

1 22. The memory system of claim 19 wherein each buffer device of the first
2 and second plurality of buffer devices each further include at least one selected from the
3 group consisting of a cache, a clock generator, and a clock alignment circuit.

1 23. A memory system comprising:
2 a controller device having an interface;
3 a first connector, second connector, and third connector;
4 a first point-to point link having a first connection to the interface and a second
5 connection to the first connector;
6 a second point-to-point link having a first connection to the interface and a second
7 connection to the second connector;
8 a third point-to-point link having a first connection to the interface and a second
9 connection to the third connector; and
10 a first memory subsystem including:
11 a buffer device having a having a first interface connected to the first
12 connector, and a second interface; and
13 a plurality of memory devices connected to the second interface.

1 24. The memory system of claim 23 wherein the second and third connectors
2 support coupling to respective second and third memory subsystems